I. In the Claims:

1. Please amend claims 1 and 6 as follows:

1 (Once Amended). A method of manufacturing an electronic device including a thin film transistor, comprising the steps of:

(a) forming a semiconductor film over an insulating substrate;

(b) depositing a first masking layer over the semiconductor film and removing portions thereof to form a plurality of holes therethrough which extend substantially perpendicularly from the upper to the lower surface thereof;

(c) patterning the first masking layer in a first pattern;

(d) depositing a second masking layer over the first masking layer;

B1 (e) patterning the second masking layer to define a second pattern that lies within the area of the first pattern; and

(f) performing an implantation in the semiconductor film using at least the first masking layer as an implantation mask to define source and drain regions, an undoped conduction channel between the source and drain regions, and a field-relief region having a lower doping concentration than the drain region between the conduction channel and the drain region.

6. (Once Amended) A method of Claim 1 wherein step (d) is carried out before step (c), and the method includes, after step (d) and before step (c), patterning the second masking layer to form a mask in the first pattern for the patterning of the first masking layer in step (c).

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Remarks

Status of the Claims

Claims 1-11 are pending in the present application. Claim 11 is the independent claim.

Rejection Under 35 USC § 102(e)

The Office Action rejects claims 1-11 under 35 USC § 102(e) in view of *Bae* (U.S. Patent 5,626,585). Applicants respectfully submit that independent claim 1 and the claims that depend directly or indirectly therefrom are patentable over the cited reference because *Bae* does not teach or suggest at least the patentable feature of claim 1 of:

"*...depositing a first masking layer over the semiconductor film and removing portions thereof to form a plurality of holes...* [and]*... performing an implantation in the semiconductor film using at least the first masking layer as an implantation mask to define source and drain regions, an undoped conduction channel between the source and drain regions, and a field-relief region having a lower doping concentration than the drain region between the conduction channel and the drain region.*"

The reference to *Bae* is drawn to the fabrication of a semiconductor device, but does not include the claimed process of depositing of a first mask and removing portions thereof to form a plurality of holes. In particular, the reference is void of a teaching of fabricating holes in a mask as the Office Action suggests. To wit, *Bae* does not teach that the removal of the photoresist 100 forms holes in the gate metal layer 54a or the buffering layer 55a, which are used as masks in a subsequent step. (Please refer to column 4, lines 11-44 of *Bae* for support for this assertion.)

Additionally, the reference to *Bae* requires two separate implant steps to form a lightly doped drain (LDD) transistor structure. The first implant step, which is used to form lightly doped source and drain regions, 56, 57, is followed by the formation of a polysilicon spacer (please refer to Figs. 3D and 3E of *Bae*) and a second implantation that forms the highly doped drain and source regions, 59, 60. The second implantation required by *Bae* uses the gate structure, which includes the etched refractory metal layer 54a, the portion 58a formed on the side walls of the refractory metal layer, and the etched polysilicon layer 53a, as the implant mask. (Please refer to column 4, lines 45-column 5, line 21 of *Bae* for support for this assertion.)

Clearly, the reference to *Bae* lacks the formation of the various regions of the electronic device recited in claim 1 in **an** implantation step, instead requiring more than one. Additionally, the reference to *Bae* lacks the teaching or suggestion of a first mask formed with a plurality of holes as is claimed.

Accordingly, and for at least the reasons set forth in detail above, it is respectfully submitted claims 1-11 are patentable over the cited reference. Accordingly, withdrawal of the 35 U.S.C. § 102(e) rejections is respectfully requested.

Conclusion

In view of the foregoing, withdrawal of all objections and rejections is respectfully requested. Allowance of all pending claims is earnestly solicited.

Except as otherwise stated in the previous Remarks, applicants note that each of the amendments have been made to place the claims in better form for U.S. practice or to clarify the meaning of the claims; not to distinguish the claims from prior art references, otherwise narrow the scope or comply with other statutory requirements. Moreover, Applicants reserve all rights they may have under the Doctrine of Equivalents.

In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact William S. Francos, Esq. (Reg. No. 38,456) at (610) 375-3513 to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and further replies to charge payment or credit any overpayment to Deposit Account Number 50-0238 for any additional fees under 37 C.F.R. §1.16 or under 37 C.F.R. §1.17.

Respectfully submitted on behalf of:
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Marked Version of Claims Showing Changes

1. A method of manufacturing an electronic device including a thin film transistor, comprising the steps of:

(a) forming a semiconductor film over an insulating substrate;

(b) depositing a first masking layer over the semiconductor film and removing portions thereof to form a plurality of holes therethrough which extend substantially perpendicularly from the upper to the lower surface thereof;

(c) patterning the first masking layer in a first pattern;

(d) depositing a second masking layer over the first masking layer;

(e) patterning the second masking layer to define a second pattern that lies within the area of the first pattern; and

(f) performing an implantation [implanting] in the semiconductor film using at least the first masking layer as an implantation mask[, with a portion of the first masking layer which defines at least some of the holes partially masking the implantation, such that the implantation defines] to define source and drain regions, an undoped conduction channel between the source and drain regions, and a field-relief region having a lower doping concentration than the drain region between the conduction channel and the drain region.

6. A method of Claim 1 wherein step (d) is carried out before step (c), and the method includes, [a further step (h)] after step (d) and before step (c), [of] patterning the second masking layer to form a mask in the first pattern for the patterning of the first masking layer in step (c).